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Agilex™ 3 FPGAs and SoCs Device Overview

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Contents

1. Overview of the Agilex™ 3 FPGAs and SoCs

The Agilex™ 3 FPGA product family extends the innovations of the Agilex FPGA portfolio to low power and cost optimized FPGA applications. The Agilex 3 FPGAs and SoCs serve a broad range of applications that require higher performance, lower power consumption, smaller form factor, and lower logic densities.

- Enhanced DSP with AI Tensor block—delivers high-efficiency artificial intelligence (AI) and digital signal processing (DSP)
- Dual-core Arm* Cortex*-A55 processors enables you to optimize the performance and power efficiency of processing workloads
- Monolithic die architecture—provides higher system integration and lower power with smaller form factor packages
- Advanced connectivity features:
  - High-speed GTS transceivers up to 12.5 Gbps
  - PCI Express* (PCIe*) 3.0 ×4 support
  - DDR external memory interface up to 2,133 Mbps LPDDR4
  - General purpose I/Os supporting voltages from 1.0 V to 3.3 V

The Agilex 3 FPGA product family delivers on average 1.9x higher fabric performance and up to 38% lower total power consumption compared to previous generation Altera FPGAs. To achieve this improvement, the product family leverages these key innovations and techniques:

- Advanced Intel® 7 technology
- Second generation Hyperflex® FPGA architecture
- High level of system integration
- Fixed low core voltage device
- Power islands, power gating, and other power reduction techniques

The Agilex 3 FPGA product family brings high performance capabilities and features to the cost optimized FPGA application space. The applications span across many segments including video and broadcast equipments, industrial, test and measurement, medical electronics, data centers, and defense.

Note: The information contained in this document is preliminary and subject to change.

Related Information

Agilex 3 FPGA and SoC FPGA on the Altera website
Provides the latest information about Agilex 3 devices.

1.1. Key Features and Innovations in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs tier consists of C-Series FPGAs.

Table 1. Agilex 3 FPGAs and SoCs C-Series

Feature and Innovation	C-Series
Process technology	Intel 7
Architecture	Monolithic die
Packaging	• Variable pitch BGA (VPBGA) package[1] for smaller form factor and to help reduce the number of PCB layers • Rectangular package and standard pattern ball array with smaller ball pitch of 0.5 mm for smaller form factor
Core fabric	Second generation Hyperflex core fabric
Logic elements	25 thousand to 135 thousand
On-chip RAM	• MLAB and M20K • 8.3 Mb
Variable precision DSP	Digital signal processing (DSP) support with up to 180 GFLOPS
AI Tensor Block	Yes
Clocking and PLL	• Programmable clock tree synthesis for flexible, low power, and low skew clocking • I/O PLL supports integer mode with precise frequency synthesis for general purpose I/O, external memory interfaces, LVDS, and fabric usage • Transmit PLL (TX PLL) supports fractional synthesis and ultra-low jitter with LC tank-based PLL for transceiver usage.
General Purpose I/Os	• 1.0 V to 1.3 V high-speed I/O (HSIO) • 1.8 V to 3.3 V high-voltage I/O (HVIO)
MIPI* D-PHY* v2.5	Up to 2.5 Gbps[2] per lane
External memory interface	Fourth generation scalable integrated hard memory controllers and PHY • 2,133 Mbps LPDDR4
Cryptographic Services	SDM supports Advanced Encryption Standard (AES)
Transceiver hard IPs	• Multiple Gigabit Ethernet (GbE) network interface connectivity in one device • PCS and PCIe hard IPs free up valuable core logic resources, save power, and increase your productivity • Hardened 10 GbE MAC, PCS, and FEC with IEEE 1588 support • Up to 12.5 Gbps NRZ • Up to PCIe 3.0 ×4

continued...

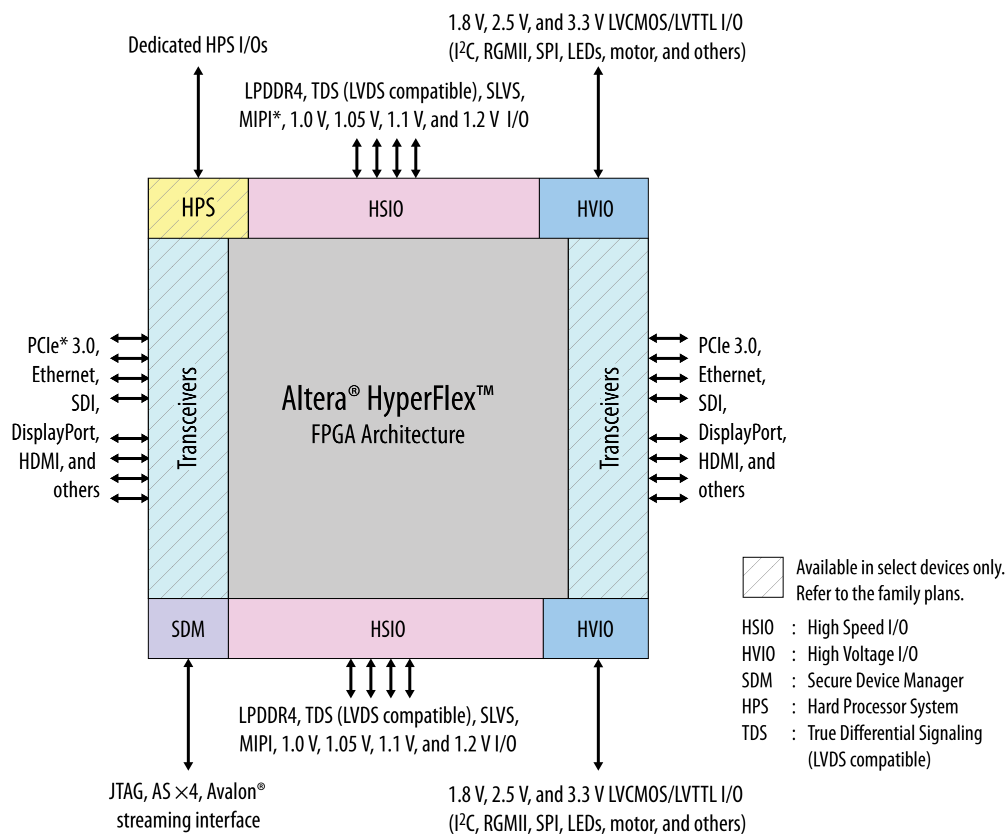
(1) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to the *PCB Design Guidelines: Agilex 3 FPGAs and SoCs*.

(2) Up to 2.5 Gbps for standard reference, short reference, and long reference channels.

Feature and Innovation	C-Series
SDM	Dedicated secure device manager (SDM) that: • Manages FPGA configuration process and all security features • Performs authenticated FPGA configuration and HPS boot • Supports FPGA bitstream encryption, secure key provisioning, and physically unclonable function (PUF) key storage • Manages runtime sensors and supports active tamper detection and responses • Supports platform attestation using the security protocol and data model (SPDM) protocol • Provides user mode access to hardened cryptographic engines as a service
HPS (SoCs only)	Hard processor system (HPS) with embedded multicore Arm processors—Dual-core 64-bit Arm Cortex-A55 up to 800 MHz
Power Saving	Comprehensive set of advanced power saving features that deliver up to 38% lower power compared to previous generation FPGAs

1.2. Agilex 3 FPGAs and SoCs Block Diagram

Figure 1. Agilex 3 FPGAs and SoCs C-Series Block Diagram



Related Information

Agilex 3 FPGAs and SoCs Family Plan on page 11

1.3. Agilex 3 FPGAs and SoCs Summary of Features

Table 2. Feature Summary

Feature	Description
Packaging	• Multiple devices with identical package footprints allows seamless migration across different device densities • Variable Pitch BGA (VPBGA) package(3) for smaller package form factor and to help reduce the number of PCB layers • 0.5 mm ball pitch package option for small form-factor with more I/O counts
High performance core fabric	• Second Generation Hyperflex core architecture with Hyper-Registers throughout the interconnect routing and at the inputs of all functional blocks • Enhanced adaptive logic module (ALM) • Improved multi-track routing architecture reduces congestion and improves compile times • Hierarchical core clocking architecture with programmable clock tree synthesis • Fine-grained partial reconfiguration
Internal memory blocks	• Multi-level on-chip memory hierarchy • M20K—20 kilobits with hard error correction code (ECC) support • MLAB—640-bit distributed LUTRAM
Variable precision DSP blocks	• Variable precision DSP blocks with hard IEEE 754-compliant floating-point units, including support for: — Single-precision FP32 (32-bit arithmetic) — Half-precision FP16 (16-bit arithmetic) and FP19 (19-bit arithmetic) floating point modes — Tensor floating point FP19 floating point modes — BFLOAT16 floating-point format • High-performance AI Tensor blocks: — Enables high-performance compute density of FPGA fabric Tera Operations Per Second (TOPS) — Up to 3.60 INT8 TOPS for AI workloads — Hardware programmable for AI with customized workloads — Supports push-button flow from industry standard frameworks, such as TensorFlow*, to FPGA bitstream • Every DSP block supports INT16 complex multiplication mode • Supports signal processing with precision ranging from 9×9 up to 54×54 • Native 27×27, 18×19, and 9×9 multiplication modes • 64-bit accumulator and cascade for systolic 200 GbE finite impulse responses (FIRs) • Internal coefficient memory banks • Pre-adder/subtractor improves efficiency • 2× additional pipeline register increases performance and reduces power consumption

continued...

(3) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to the *PCB Design Guidelines: Agilex 3 FPGAs and SoCs*.

Feature		Description
Core clock networks		• Programmable clock tree synthesis—backwards compatible with global, regional and peripheral clock networks • Synthesize clocks where needed only—minimizes dynamic power • 625 MHz LVDS interface clocking—supports 1,250 Mbps LVDS interface through the 1.3 V TDS standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 1,067 MHz external memory interface clocking, supports 2,133 Mbps LPDDR4 interface
General purpose I/Os	General	• 1.25 Gbps 1.3 V TDS standard compatible with LVDS, RSDS, mini-LVDS, and LVPECL standards • 1.0 V, 1.05 V, 1.1 V, and 1.2 V single-ended LVCMOS interfacing • 1.8 V, 2.5 V, and 3.3 V single-ended LVCMOS/LVTTL I/O • On-chip termination (OCT) • Over 300 total GPIOs available
	External memory interface (Hard IP)	1,067 MHz (2,133 Mbps) LPDDR4 external memory interface
	MIPI	MIPI D-PHY v2.5 at up to 2.5 Gbps(4) per lane
Phase locked loops (PLL)	I/O PLL	• Integer PLLs adjacent to general purpose I/Os • Precision frequency synthesis • Clock delay compensation • Zero-delay buffering • Support external memory and LVDS-compatible interface
	Transmit PLLs (TX PLLs)	• Precise fractional synthesis • Ultra low jitter with LC tank-based PLL • Supports transceiver interfaces
	System PLL	• One System PLL per GTS transceiver bank • Integer mode • Precision frequency synthesis • Supports transceiver-to-fabric interface • You can repurpose the System PLL for core usage if it is not used by the GTS transceiver
Memory controller support		Multiple hard IP instantiations in each device • LPDDR4 hard memory controller
Transceivers	PCIe	PCIe rates up to PCIe 3.0, 8 Gbps NRZ
	Networking	• Oversampling capability for data rates below 1 Gbps • SFP+ optical module support • Adaptive linear and decision feedback equalization • Transmit pre-emphasis and de-emphasis • Dynamic reconfiguration of individual GTS transceiver channels • On-chip instrumentation (Quartus® Prime Eye Viewer with non-destructive eye height and destructive eye width margining) • Continuous operating range of 1 Gbps to 12.5 Gbps NRZ

continued...

(4) Up to 2.5 Gbps for standard reference, short reference, and long reference channels.

Feature		Description
Transceiver hard IP	PCIe	• One hard IP instantiations in each device • Single-root I/O virtualization (SR-IOV) • Precise time management • Up to PCIe 3.0 ×4 EP and RP
	Other protocols	• CR/KR (AN/LT) • 1588 PTP • MAC, PCS, and FEC bypass options • Ethernet IP configuration: 10GE-1 MAC, PCS, and FEC
Configuration		• Dedicated SDM • Software-programmable device configuration • Serial flash interface • Configuration from parallel flash through external host • Fine-grained partial reconfiguration of core fabric—add or remove system logic while the device is operating • Dynamic reconfiguration of GTS transceivers and PLLs • Comprehensive set of security features including AES-256, SHA-256/384, and ECDSA-256/384 accelerators • PUF service • Platform attestation • Anti-tamper features • Configuration via protocol (CvP) using PCIe 1.0, 2.0, or 3.0
Functional safety		• Functional Safety Data Package (FSDP) • Improved FPGA diagnostic measures enable use of Agilex 3 FPGAs in safety-critical applications
Software and tools		• Quartus Prime Pro Edition design suite with new compiler and Hyper-Aware design flow • New compile innovations in each Altera® oneAPI release • Transceiver toolkit • Platform Designer IP integration tool • Altera DSP Builder for Altera FPGAs advanced blockset • Arm Development Studio for Altera SoC FPGA (Arm DS for Altera SoC FPGA)

1.4. Additional Features for Agilex 3 SoCs

In addition to the common features of the Agilex 3 FPGAs and SoCs, the Agilex 3 SoCs provide additional features.

Table 3. Features Specific to Agilex 3 SoCs

SoC Subsystem	Feature	Description
HPS	Multiprocessor unit core	• Dual-core Arm Cortex-A55 MPCore processors, with Arm CoreSight* debug and trace technology • Scalar floating-point unit supporting single and double precision • Arm Neon* technology media processing engine for each processor
	System controllers	• System memory management unit (SMMU) • Cache coherency unit (CCU)

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SoC Subsystem	Feature	Description
	Cache	• Arm Cortex-A55: — Level 1 cache per core: • 32 KB L1 instruction cache with parity • 32 KB L1 data cache with ECC — Level 2 cache per core: Unified 128 KB L2 data and instructions cache with ECC • Level 3 cache: 1 megabytes (MB) L3 cache
	On-chip memory	512 KB on-chip RAM
	Direct memory access (DMA)	Eight-channel DMA controller
	Ethernet MAC (TSN)	Three 10 Mbps/100 Mbps/1 Gbps Ethernet MACs with integrated DMA and Time-Sensitive Networking (TSN) support
	USB	• One USB 2.0 On-The-Go (OTG) with integrated DMA • One USB 3.1 Gen 1
	UART	Two UART 16550-compatible controllers
	Serial peripheral interface (SPI) controller	Four SPI (two masters and two slaves)
	I^{2}C	Five I^{2}C controllers
	I^{3}C	Two I^{3}C controllers
	SD/SDIO/eMMC controller	• SD/eMMC devices up to version 5.1 • SD devices up to version 6.1 • SDIO devices up to version 4.1
	NAND flash controller	• One ONFI 1.x and 2.x • 8 bit and 16 bit support • Compatible with Toggle 1.x and 2.x specifications
	GPIO	Maximum of 48 software-programmable GPIOs
	Timers	• Four general-purpose timers • Five watchdog timers
SDM		• Secure boot • AES encryption • Secure Hash Algorithms (SHA) and Elliptic Curve Digital Signature Algorithm (ECDSA) authentications • Supports post quantum cryptography (PQC) native boot
External memory interface		Hard memory controllers—LPDDR4

2. Agilex 3 FPGAs and SoCs Family Plan

The Agilex 3 FPGAs and SoCs are available as C-Series FPGAs with different features to fit your application requirements.

Note:
- The tables in the following sections are preliminary and subject to change.
- The resource counts vary by package options.
- The performance specifications vary by speed grades.
- The HPS and GTS transceivers are available only for specific ordering part numbers.

Related Information

Agilex 3 FPGAs and SoCs Family Plan on page 11

2.1. Agilex 3 FPGAs and SoCs C-Series

Table 4. C-Series FPGA Family Plan—Core Features

The values in this table are maximum resources or performance.

Device	Logic Element	Adaptive Logic Module	M20K		MLAB		DSP	
			Count	Size (Mb)	Count	Size (Mb)	18×19 Multipliers	Peak INT8 (TOPS[5])
A3C 025	25,075	8,500	65	1.27	450	0.27	68	0.67
A3C 050	47,200	16,000	123	2.40	800	0.49	130	1.27
A3C 065	65,490	22,200	169	3.30	1,050	0.64	176	1.72
A3C 100	100,300	34,000	262	5.12	2,000	1.22	276	2.70
A3C 135	135,110	45,800	353	6.89	2,300	1.40	368	3.60

(5) Tera Operations Per Second

Table 5. C-Series FPGA Family Plan—I/Os and Interfaces

The values in this table are maximum resources or performance.

Device	HVIO (1.8 V–3.3 V)	HSIO (1.0 V–1.3 V)	PLL Count		1.3 V LVDS Pairs at 1.25 Gbps	LPDDR4 Interface (×32)	MIPI D-PHY Interface
			I/O PLL(6)	System PLL(7)			
A3C 025	160	96	7	0	48	0	7
A3C 050	160	96	7	0	48	1	7
A3C 065	160	96	7	0	48	1	7
A3C 100	200	192	11	1	96	2	14
A3C 135	200	192	11	1	96	2	14

Table 6. C-Series FPGA Family Plan—Transceivers and HPS

The values in this table are maximum resources or performance.

Device	PCIe 3.0 ×4	HPS	
		Processor	Cache Size
A3C 025	—	—	—
A3C 050	—	—	—
A3C 065	—	—	—
A3C 100	1	• Dual core Arm Cortex-A55 up to 800 MHz	• Shared: 1 MB L3 • Cortex-A55: — 32 KB L1 — 128 KB L2
A3C 135	1		

(6) I/O PLL includes I/O bank I/O PLLs and fabric-feeding I/O PLLs.

(7) You can repurpose the System PLL for core fabric usage if you do not use it for transceiver.

2.2. Agilex 3 FPGAs and SoCs C-Series Package Options

Figure 2. Package Options, Migrations, and I/O Pins—C-Series

In this figure, the arrows indicate the package migration paths. The shades represent the devices included in each path.

Series	Device	Package Key: HVIO / HSIO (LVDS) / HPSIO / Transceivers				
		Ball Pitch: 0.5 mm Grid Array Pattern: Standard MBGA: Micro Fineline BGA		Ball Pitch: Variable (1)(2) Grid Array Pattern: Variable Pitch BGA VPBGA: Variable Pitch BGA		
		M12A 484-pin MBGA 12 mm × 12 mm	**M16A** 896-pin MBGA 16 mm × 16 mm	**B18A** 474-pin VPBGA 18 mm × 18 mm	**B18B** 538-pin VPBGA 23 mm × 23 mm	**B23C** 931-pin VPBGA 23 mm × 23 mm
C-Series	A3C 025	160 / 96 (48) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
	A3C 050	160 / 96 (48) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
	A3C 065	160 / 96 (48) / 0 / 0		160 / 48 (24) / 0 / 0	160 / 96 (48) / 0 / 0	
	A3C 100		40 / 192 (96) / 48 / 4	160 / 48 (24) / 0 / 0		200 / 144 (72) / 48 / 4
	A3C 135		40 / 192 (96) / 48 / 4	160 / 48 (24) / 0 / 0		200 / 144 (72) / 48 / 4

Notes:
(1) The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias.
(2) The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to PCB Design Guidelines: Agilex™ 3 FPGAs and SoCs.

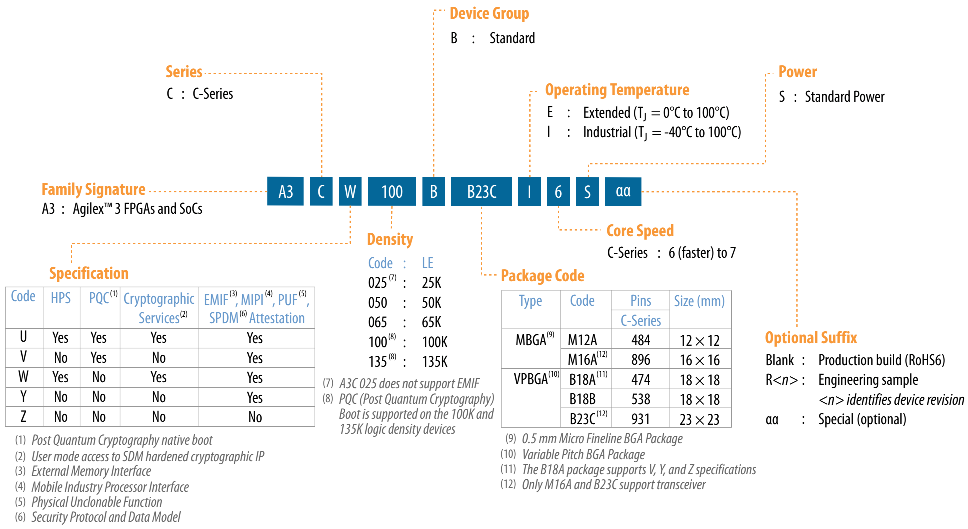
For more information about the device migration path, refer to the *Device Migration Guidelines: Agilex 3 FPGAs and SoCs C-Series*.

Related Information

- PCB Design Guidelines: Agilex 3 FPGAs and SoCs
  Provides more information about the device migration path.
- Device Migration Guidelines: Agilex 3 FPGAs and SoCs C-Series
  Provides more information about the device migration path.

2.3. Part Number Decoder

Figure 3. Agilex 3 FPGAs and SoCs Ordering Part Number



3. Second Generation Hyperflex Core Architecture

The Agilex 3 FPGAs and SoCs are based on a core fabric featuring the second generation Hyperflex core architecture.

Table 7. Advantages of the Hyperflex Core Architecture

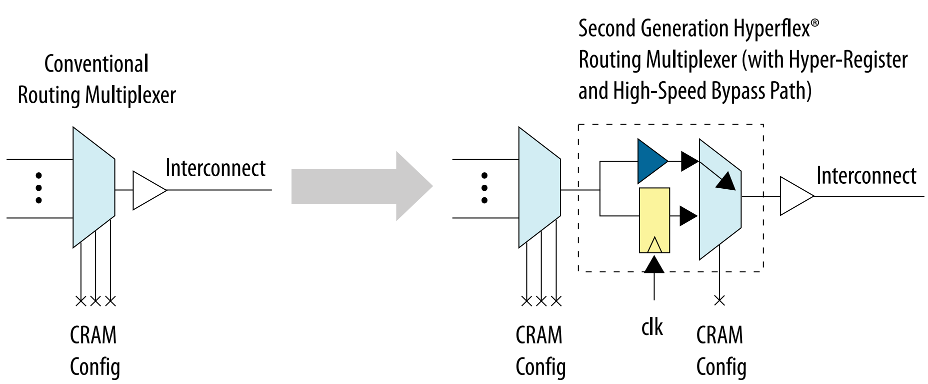
This table lists some of the advantages of the Hyperflex core architecture.

Advantage	Description
Higher throughput	Delivers, on average, 1.9x higher core clock frequency performance in designs from previous generation FPGAs to obtain throughput breakthroughs.
Improved power efficiency	Uses reduced IP size to consolidate designs that previously spanned multiple devices into a single device.
Greater design functionality	Uses faster clock frequency to reduce bus widths and reduce IP size. The reduced bus widths and IP size free up additional FPGA resources to add greater functionality.
Increased designer productivity	Boosts performance with less routing congestion and fewer design iterations using the Hyper-Aware design tools, obtaining greater timing margin for more rapid timing closure.

Additional to traditional ALM user registers, the Hyperflex core architecture adds bypassable registers called Hyper-Registers:

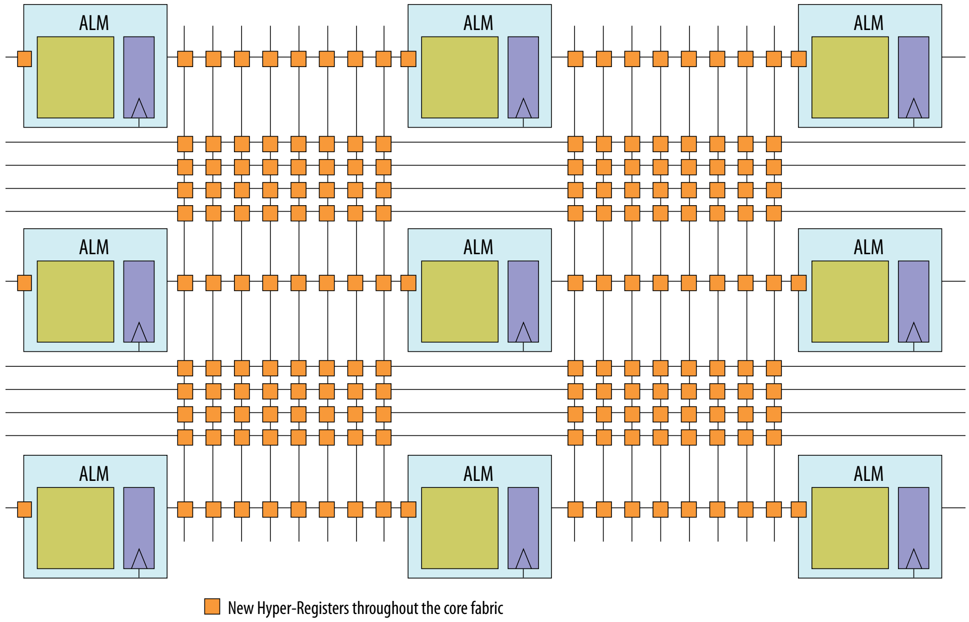
- Distributed throughout the FPGA fabric.
- Available on every interconnect routing segment and at the inputs of all functional blocks.

Figure 4. Bypassable Hyper-Register



In the second generation Hyperflex core architecture, Altera optimized the number of registers to improve timing closure time and fabric area utilization.

Figure 5. Hyperflex Core Architecture



The Hyper-Registers enable you to achieve core performance increases using key design techniques. If you implement these design techniques, the Hyper-Aware design tools automatically utilizes the Hyper-Registers to achieve maximum core clock frequency:

- Fine grain Hyper-Retiming to eliminate critical paths
- Zero-latency Hyper-Pipelining to eliminate routing delays
- Flexible Hyper-Optimization for best-in-class performance

4. Adaptive Logic Module in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs use an enhanced adaptive logic module (ALM) as shown in the *ALM Block Diagram* figure and its key features and capabilities are listed in the *Key Features and Capabilities of the ALM* table.

Figure 6. ALM Block Diagram

This figure shows the ALM with 8-input fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

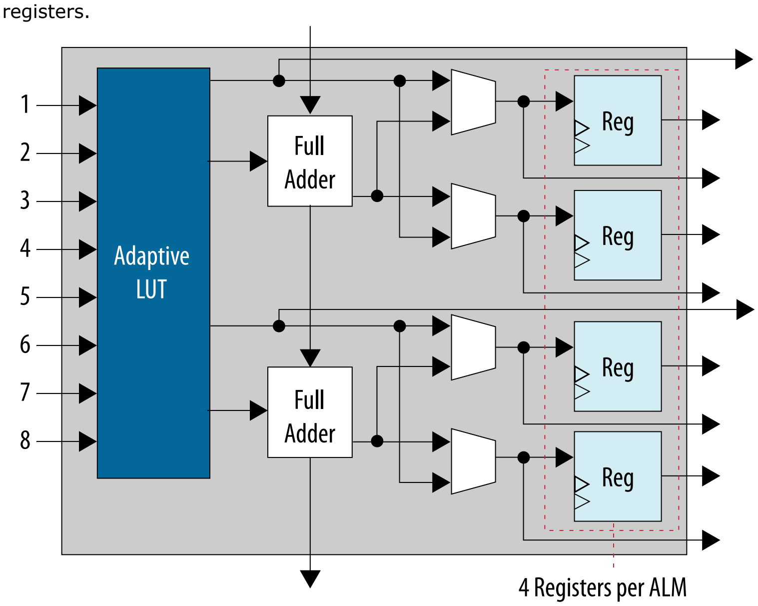


Table 8. Key Features and Capabilities of the ALM

Key Feature	Capability
High register count	Together with the second generation Hyperflex architecture, the four registers per 8-input fracturable LUT enables maximized core performance at very high core logic utilization.
ALM operating modes	Optimize core logic utilization by implementing an extended 7-input logic function, a single 6-input logic function, or two smaller independent functions (for example, two 4-input functions).
Two clock sources	Two clock sources per ALM generate two normal clocks and two delayed clocks to drive the ALM registers, resulting in more clock domains and time-borrowing capability.
Additional LUT outputs	Additional fast 6-LUT and 5-LUT outputs for combinatorial functions improve critical path for logic cascade.
Improved register packing	The improved register packing, including 5-input LUT with two packed register paths, results in more efficient usage of the fabric area and improved critical path.
Latch mode support	The ALM supports latch mode in the address latch enable.

The Quartus Prime software capitalizes on the ALM logic structure to deliver the highest performance, optimal logic utilization, and lowest compile times. The Quartus Prime software simplifies design reuse as the software automatically maps legacy designs into the ALM architecture of the Agilex 3 FPGAs and SoCs.

5. Internal Embedded Memory in Agilex 3 FPGAs and SoCs

The embedded memory blocks in Agilex 3 FPGAs and SoCs are similar to the embedded memory of previous generation Altera FPGAs.

Table 9. Embedded Memory Block Types and Features for Agilex 3 FPGAs and SoCs

Feature	MLAB	M20K
Usage	For wide and shallow memory configurations	For supporting larger memory configurations
Block size	640 bits	20 kilobits
Configurations	• 64×10 (emulated) • 32×20	• 2,048×10 (or ×8) • 1,024×20 (or ×16) • 512×40 (or ×32)
Hard ECC	—	Yes
Modes	Single-port RAM, dual-port RAM, FIFO, ROM, and shift register	

6. Variable-Precision DSP in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs are the cost-optimized FPGAs with an AI tensor block, making it the ideal choice for edge AI applications.

For INT8 operations in a single DSP block, the Agilex 3 FPGAs and SoCs C-Series improve peak theoretical TOPS up to 5.1 times than Cyclone® V FPGAs.

Through a large increase in arithmetic density[8], the Agilex 3 FPGAs and SoCs fit more multipliers and accumulators in the same footprint of a standard DSP block.

The FPGA AI Suite (FPGA AI) supports the new AI features. The FPGA AI Suite enables push-button flow from industry standard frameworks—such as Caffe, PyTorch*, and TensorFlow—to FPGA bitstream.

Additionally, the Agilex 3 FPGAs and SoCs also carry over the variable-precision DSP architecture from previous Altera FPGAs with hard fixed point and IEEE 754-compliant floating point capabilities.

In fixed point mode, you can configure the DSP blocks to support signal processing with precisions from 9×9 up to 54×54:

- Increased 9×9 multipliers count, with three 9×9 multipliers for every 18×19 multiplier
- A pipeline register increases the maximum DSP block operating frequency and reduces the power consumption
- Dynamically switch multiplier inputs through `scanin` and `chainout` signals
- Compile each DSP block independently as six 9×9, dual 18×19, or single 27×27 multiply-accumulate.

The variable-precision DSP supports floating point addition, multiplication, multiply-add, and multiply-accumulate:

- Single-precision 32-bit arithmetic FP32 floating point mode
- Half-precision 16-bit arithmetic FP16 and FP19 floating point modes, and BFLOAT16 floating point format

With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to efficiently implement even higher-precision DSP functions.

(8) Arithmetic density is a measure of how many dot products can fit into a 1 mm^2 of silicon on any given process node.

Table 10. Variable-Precision DSP Block Configurations in Agilex 3 FPGAs and SoCs C-Series

This table lists the way Agilex 3 FPGAs and SoCs C-Series accommodate the different precisions within a DSP block or by utilizing multiple DSP blocks.

Multiplier	DSP Block Resource Usage	Expected Application
9×9 bits	One-sixth of a variable-precision DSP block (One DSP block can support six 9×9)	Low-precision fixed point
18×19 bits	Half of a variable-precision DSP block	Medium-precision fixed point
27×27 bits	One variable-precision DSP block	High-precision fixed point
19×36 bits	One variable-precision DSP block with external adder	Fixed point fast Fourier transform (FFT)
36×36 bits	Two variable-precision DSP blocks with external adder	Very high-precision fixed point
54×54 bits	Four variable-precision DSP blocks with external adder	Double-precision fixed point
Half-precision floating point	One variable-precision DSP block (Contains adder for two FP16, FP19, or BFLOAT16 multipliers with one accumulator)	Half-precision floating point
Single-precision floating point	One variable-precision DSP block (Contains one FP32 multipliers with one accumulator)	Single-precision floating point
AI tensor block	Two sums of ten INT8×INT8 multipliers tensor fixed-point and floating-point computation	Tensor dot products of 10-element vectors computation
Complex multiplication mode	One variable-precision DSP block (16×16 ± 16×16)	INT16 complex multiplication

7. Core Clock Network in Agilex 3 FPGAs and SoCs

Agilex 3 FPGAs and SoCs use programmable clock tree synthesis for its core clocking function.

Programmable clock tree synthesis uses dedicated clock tree routing and switching circuits. These dedicated circuits enable the Quartus Prime software to create the exact clock trees that your design requires.

Advantages of using programmable clock tree synthesis:

- Minimizes clock tree insertion delay
- Reduces dynamic power dissipation in the clock tree
- Allows greater flexibility of clocking in the core
- Maintains backwards compatibility with legacy global and regional clocking schemes

Features of the core clock network of Agilex 3 FPGAs and SoCs:

- Supports the second-generation Hyperflex core architecture
- Supports the hard memory controllers[9] for:
  — LPDDR4—up to 2,133 Mbps
- Supported by dedicated clock input pins and integer I/O PLLs

Related Information

- Key Features and Innovations in Agilex 3 FPGAs and SoCs on page 5
- Agilex 3 FPGAs and SoCs Summary of Features on page 7

(9) Each Agilex 3 FPGA series has different hard memory controller support. For more information, refer to the related information.

8. I/O PLLs in Agilex 3 FPGAs and SoCs

The I/O banks of the Agilex 3 FPGAs and SoCs contain I/O PLLs for use in I/O interfacing or fabric clocking.

Table 11. I/O PLLs in Different I/O Bank Types

I/O Bank Type	Bank I/O PLL	Fabric-Feeding I/O PLL
HSIO (96 I/Os)	2	1
HVIO (2×20 I/Os)	—	1

You can use the I/O PLLs for general purpose applications in the core fabric, such as clock network delay compensation and zero-delay clock buffering.

The I/O PLLs are situated adjacent to the hard memory controllers and LVDS serializer/deserializer (SERDES) blocks in the I/O bank. This placement creates a tight coupling of the PLLs with the I/Os that need them. The architecture simplifies designing external memory and high-speed LVDS interfaces, and eases timing closure.

9. General Purpose I/Os in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs are equipped with two types of general purpose I/Os—the high-speed I/Os (HSIO) and the high-voltage I/Os (HVIO). Both HSIO and HVIO enable important support for edge applications in Agilex 3 FPGAs and SoCs.

Table 12. I/O Standards Support and Performance

I/O Type	I/Os Per Bank	I/O Standard	Specification	Notes
HSIO	96(10)	LVCMOS	1.0 V, 1.05 V, 1.1 V, and 1.2 V single-ended	—
		TDS (LVDS compatible)	• 1.3 V • Up to 1.25 Gbps	Works with the LVDS SERDES IP
		MIPI D-PHY	• Version 2.5 • Up to 2.5 Gbps(11) (high speed and low power mode)	Supports up to eight data lanes: • 1D+C • 2D+C • 4D+C • 8D+C
		SGMII (TDS (LVDS compatible))	Up to 1.25 Gbps	If required, add AC coupling
HVIO	20	LVCMOS/ LVTTL	• 1.8 V single-ended • 0.250 Gbps (125 MHz DDR)	RGMII support at 1.8 V
			• 2.5 V/3.3 V single-ended • 0.200 Gbps (100 MHz DDR)	

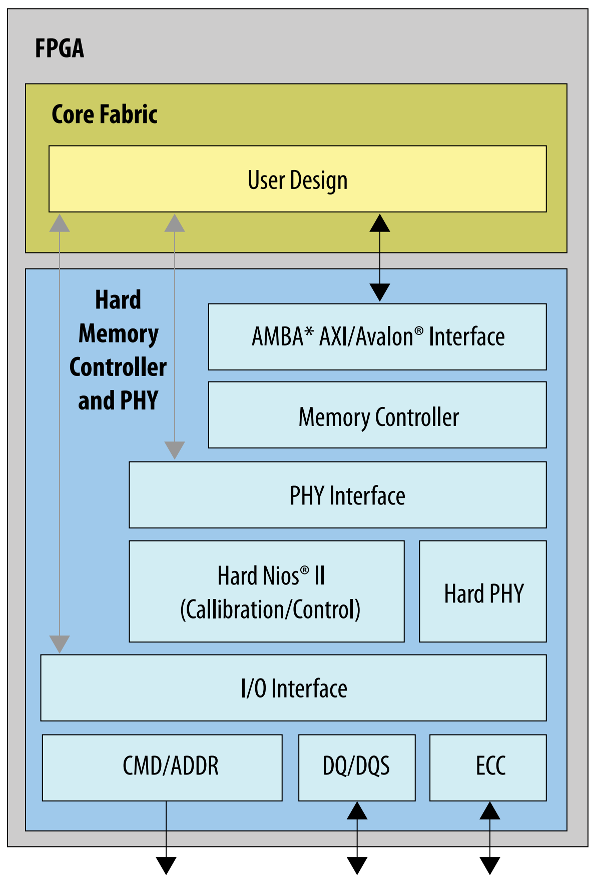
(10) There are two sub-banks in each HSIO bank. Each sub-bank is powered by its own V_{CCIO}.

(11) Up to 2.5 Gbps for standard reference, short reference, and long reference channels.

10. External Memory Interface in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs feature a substantial external memory bandwidth. This bandwidth is accompanied by the ease-of-design, lower power, and resource efficiencies of high-performance hard memory controllers. Using the hard or soft memory controller, you can configure external memory interfaces width up to a maximum of 32 bits.

Figure 7. Hard Memory Controller



Each I/O bank contains 96 general purpose I/Os and two high-efficiency hard memory controllers. The hard memory controllers support various memory types, each with different performance capabilities. You can bypass the hard memory controller and implement a soft memory controller in user logic.

Each I/O contains a hard DDR read and write path (PHY) capable of performing key memory interface functions such as:

- Read and write leveling
- FIFO buffering to lower latency and improve margin
- Timing calibration
- On-chip termination

Hard microcontrollers aid the timing calibration. Altera customized these hard microcontrollers to control the calibration of multiple memory interfaces. The calibration enables the Agilex 3 device to compensate for process, voltage, and temperature (PVT) variance within the Agilex 3 device or the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

10.1. External Memory Interface Performance

Table 13. C-Series FPGAs External Memory Interface Performance

Interface Protocol	Memory Controller	Interface Performance (Mbps)	Maximum Width (Bits)
LPDDR4	Hard	2,133	32

10.2. Features of the Hard Memory Controller

Table 14. Hard Memory Controller Features

Feature	Description
Protocol	LPDDR4—up to two chip selects
Interface	• Fully pipelined command, read, and write data interfaces to the controller • Arm AMBA* 4 AXI compliance including AXI ordering rules: — Four priority quality of service (QoS) levels — Programmable address mapping — Exclusive monitors
Scheduling	• Software-configurable priority scheduling on individual SDRAM bursts • Advanced bank look-ahead features for high memory throughput • Configurable for one of these placement orders: — Out-of-order placement for writes — In-order placement for writes from the same port — In-order placement for writes from the same AXI master • Configurable for in-order scheduling for reads and writes • Support read or write grouping
Timing	Fully programmable timing parameter support for all JEDEC*-specified timing parameters
Refresh	All bank refresh or per bank refresh (if supported by memory)
ECC	• Error correction code (ECC) support including calculation, error correction, write-back correction, and error counters • Hardened ECC support including configurations for various ECC types with programmable single-bit and double-bit error reporting and automatic correction: — In-line ECC or no ECC — Supports standard single bit error correction and double bit error detection — Supports scrubbing

continued...

Feature	Description
Power states	Low power DRAM states including active power down, precharge power down, and self-refresh power down states for DRAM: • Under register control; or • Based on idle times
Training	Initial and periodic ZQ calibration (LPDDR4)
Verification	• Performance monitoring statistics • Memory test for DDR memories through register control

11. Hard Processor System in Agilex 3 SoCs

The Agilex 3 SoCs hard processor system (HPS) consists of dual-core Arm Cortex-A55 processors. Additionally, the HPS adds a system memory management unit that enables system-wide hardware virtualization.

With the HPS architecture improvements, the Agilex 3 SoCs fulfill the requirements of current and future embedded markets, including:

- Wireless and wireline communications
- Datacenter acceleration
- Various industrial applications

Figure 8. Agilex 3 SoCs HPS Block Diagram

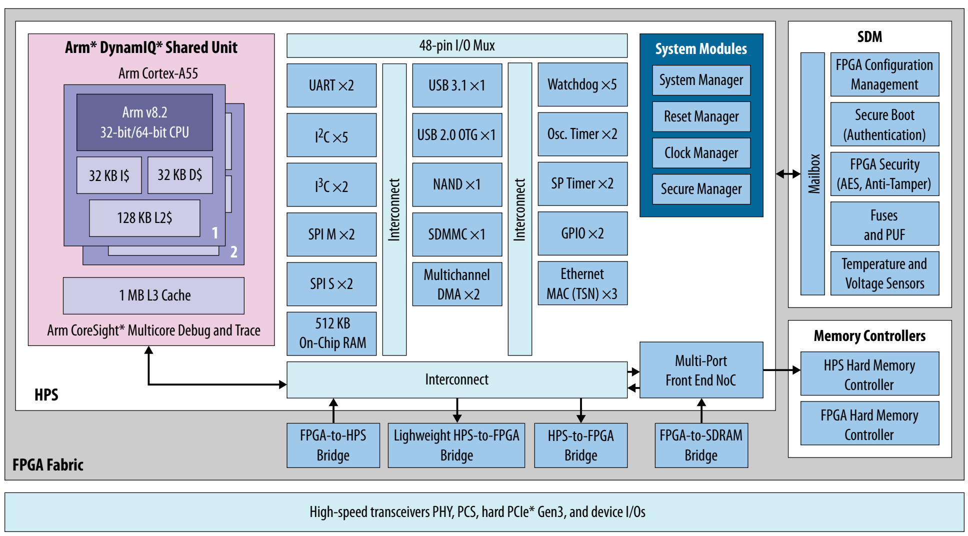


Table 15. Summary of Agilex 3 SoCs Key Features

Feature	Description
Processor units	• Dual-core Arm Cortex-A55 MPCore processor units — CPU frequency: Dual-core Arm Cortex-A55—up to 800 MHz — Arm v8.2-A architecture • Run 64-bit and 32-bit Arm instructions • 16-bit and 32-bit Thumb instructions for 30% reduction in memory footprint • Arm Jazelle* runtime compilation target (RCT) execution architecture with 8-bit Java* bytecodes • Superscalar, variable-length, out-of-order pipeline with dynamic branch prediction

continued...

Feature		Description
		• Improved Arm Neon media processing engine • Single-precision and double-precision floating-point unit • Arm CoreSight debug and trace technology
System memory management unit		• Enables a unified memory model • Extends hardware virtualization into peripherals implemented in the FPGA fabric
Cache coherency unit		Propagates changes in shared data stored in cache throughout the system to provide I/O coherency for co-processing elements
Cache memory	Common	Shared 1 MB L3 cache
	Dual-core Arm Cortex-A55	• 32 KB L1 I-cache and 32 KB L1 D-cache with ECC per core • 128 KB unified L2 data and instructions cache per core
On-chip memory		512 KB on-chip RAM
External SDRAM and flash memory Interfaces for HPS	Hard memory controller	• Supports LPDDR4 • 40-bit (32-bit + 8-bit ECC) • ECC support including calculation, error correction, write-back correction, and error counters • Software-configurable priority scheduling on individual SDRAM bursts • Fully programmable timing parameter support for all JEDEC-specified timing parameters • Multi-port front end (MPFE) interface to the hard memory controller, supporting AMBA 4 AXI QoS for interface to the FPGA fabric
	NAND flash controller	• Integrated descriptor-based controller with DMA • Programmable hardware ECC support • Support for 8-bit and 16-bit flash devices • Compatible with the ONFI 1.x and 2.x specifications • Compatible with Toggle 1.x and 2.x specifications
	SD/SDIO/eMMC controller	• Integrated descriptor-based DMA controller • Supports CE-ATA digital commands • Supports SD devices up to version 6.1 • Supports SDIO devices up to version 4.1 • Supports SD/eMMC devices up to version 5.1 • Supports SD SDR12, SDR25, SDR50, and SDR104 • Supports eMMC legacy, high-speed SDR, high-speed DDR, HS200, and HS400 • Does not support UHS-II and UHS-III interfaces
	DMA controller	• Two controllers with four channels each • Supports up to 48 peripheral handshake interfaces

continued...

Feature		Description
Communication interface controllers	Ethernet MAC	• Three Ethernet MACs supporting 10 Mbps, 100 Mbps, and 1 Gbps with integrated DMA and TSN support • Ethernet standards with TSN endpoint functionality compliant to: — IEEE 1588-2008 advanced timestamps: Precision Time Protocol (PTP), 2-steps, PTP offload and timestamping — IEEE 802.1AS: Timing and synchronization — IEEE 802.1Qav: Time-sensitive streams forwarding and queuing — IEEE 802.1Qbv: Time-scheduled traffic enhancements — IEEE 802.1Qbu: Frame pre-emption — IEEE 802.3br: Interspersing express traffic • Ethernet interfaces: — Supports RGMII operating mode at 10 Mbps, 100 Mbps, and 1 Gbps data rates through HPS I/O — Supports RGMII operating modes at 10 Mbps, 100 Mbps, and 1 Gbps data rates through FPGA HVIO with GMII–to–RGMII soft adapter in FPGA logic — Supports SGMII+ operating mode at 10 Mbps, 100 Mbps, and 1 Gbps data rates with SGMII+ PCS soft IP and serial transceiver interface through FPGA I/O — Supports SGMII operating mode at 1 Gbps (1000BASE-X) or 10 Mbps, 100 Mbps, and 1 Gbps (SGMII) data rates with SGMII PCS soft IP through TDS I/O (LVDS compatible)
	USB 2.0 OTG	• One USB OTG controller • Dual-role device (device and host functions) — High-speed (480 Mbps) — Full-speed (12 Mbps) — Low-speed (1.5 Mbps) — Supports USB 1.1 (full-speed and low-speed) • Integrated descriptor-based scatter-gather DMA • Support for external ULPI PHY • Up to 16 bidirectional endpoints, including control endpoint • Up to 16 host channels • Supports generic root hub • Configurable to USB OTG 1.3 and USB OTG 2.0 modes
	USB 3.1 Gen1	• Supports both device and host controller modes — Both USB 3.1 and USB 2.0 interfaces must be configured as device or host; mixing modes is not supported • Supports up to 5 Gbps if configured for USB 3.1 Gen1 and interfaced with the transceiver • Supports up to 480 Mbps if configured for USB 2.0 and interfaced with the HPS I/O
	I^{2}C	• Five I^{2}C controllers, three can be used by the Ethernet MAC for MIO to external PHY • Support 100 Kbps and 400 Kbps modes • Support 7-bit and 10-bit addressing modes • Support master and slave operating modes
	I^{3}C	• Two I^{3}C controllers • — One configured as the primary master — One configured as the secondary master • Supports FM, FM+, and SDR data rates up to 12.5 Mbps
	UART	• Two UART 16550-compatible controllers • Programmable baud rate up to 115.2 kilobaud
	SPI	• Four SPI (two masters, two slaves) • Supports full duplex and half duplex

continued...

Feature		Description
Timers		• Four general-purpose timers • Five watchdog timers
I/O		• 48 HPS direct I/Os allow HPS peripherals to connect directly to the I/Os • Up to two FPGA fabric I/O banks assignable to the HPS for HPS DDR access
Interconnect to logic core	HPS–to–FPGA bridge	• Allows HPS bus masters to access bus slaves in FPGA fabric • Configurable 32-, 64-, or 128-bit AMBA AXI data interface allows high-bandwidth HPS master transactions to FPGA fabric • Supports up to 256 gigabytes (GB) of address space
	Lightweight HPS–to–FPGA bridge	• Lightweight 32-bit AMBA AXI interface suitable for low bandwidth register access from HPS to soft peripherals in the FPGA fabric • Supports up to 512 MB of address space
	FPGA–to–HPS bridge	• 256 bits FPGA–to–HPS interface targeting the HPS peripherals and shared SDRAM • Shared SDRAM accessible using non-coherent(12) or hardware-supported I/O coherent transactions • Supports ACE5-Lite cache stashing into L3 cache of the DynamIQ Shared Unit or L1 cache of individual core
	FPGA–to–SDRAM bridge	• 64, 128, or 256 bits FPGA–to–SDRAM interface targeting the DDR I/O • Supports only non-coherent(12) transactions

(12) For non-coherent transactions, ensure that the HPS and FPGA soft logic do not interfere in the SDRAM space of each other.

12. Transceivers in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs are equipped with NRZ transceivers optimized for a wide variety of applications, ranging from 1 Gbps to 12.5 Gbps NRZ.

The monolithic GTS transceivers in Agilex 3 FPGAs and SoCs enable low latencies for edge or mid-range FPGA applications. For long reach backplane-driving applications, the devices use advanced adaptive equalization circuits to equalize system loss.

All Agilex 3 FPGA GTS transceiver channels are equipped with these blocks:

- Dedicated PMA—provides primary interfacing capabilities to physical channels.
- Hardened PCS—supports 64b/66b encoding and decoding functions, data scrambling, block alignment, and gearboxing functions.
- FEC—Firecode FEC for 10 GbE BASE-KR/CR applications and Reed Solomon FEC.

A single PMA–PCS channel with independent clock domains forms each GTS transceiver channel. Using a highly configurable clock distribution network, you can configure various bonded and non-bonded data rate within each GTS transceiver bank.

Figure 9. C-Series FPGAs GTS Transceiver Block Diagrams

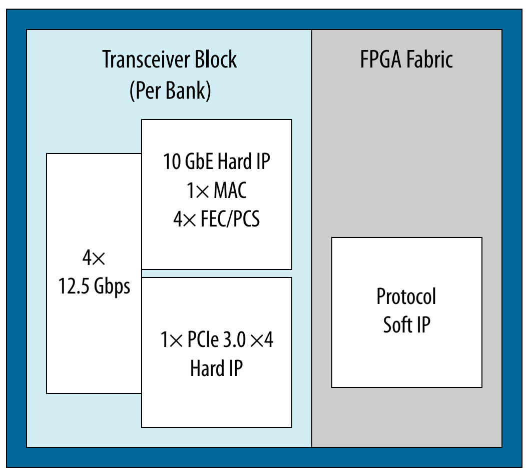


Table 16. Capabilities of FPGA GTS Transceivers in Agilex 3 FPGAs and SoCs

Capability	Maximum Specification
	C-Series FPGA
Maximum speed	12.5 Gbps NRZ (1–12.5 Gbps continuous)
FEC	10 GbE FEC direct mode (IEEE 802.3 Clause 74 Firecode FEC hard IP)
PCS	10 GbE PCS direct mode[(13)] (64b/66b hard IP)
PCIe	Up to PCIe 3.0 ×4 controller hard IP
Transmitter/ Receiver	Independent transmitter and receiver to support combining simplex protocols
PMA	PMA direct mode (bypass Ethernet and PCIe hard IPs)

12.1. PMA Features in Agilex 3 FPGA GTS Transceivers

The transmitter, receiver, and high speed clocking resources form the PMA channels. The transmit features deliver exceptional signal integrity at data rates up to 12.5 Gbps NRZ. Additionally, each PMA features advanced equalization circuits that compensate for transmission losses across a wide frequency spectrum.

Table 17. GTS Transceiver PMA Features in Agilex 3 FPGAs and SoCs

Feature	Capability
Data rates	Up to 12.5 Gbps
Optical module support	SFP+ optical module support
Cable driving support	SFP+ Direct Attach
Transmit pre-emphasis	One post-tap and two pre-taps for NRZ
Dynamic reconfiguration	Independent control of each GTS transceiver channel Avalon® memory-mapped interface for transceiver flexibility
Multiple PCS–PMA and PCS to FPGA fabric interface widths	• Flexible deserialization width, encoding, and reduced latency • GTS transceiver (PMA with optional FEC or PCS) to FPGA fabric interface—from 8 bits up to 66 bits options

12.2. PCS Features in Agilex 3 FPGA GTS Transceivers

The PMA channels in the Agilex 3 FPGAs and SoCs interface with the core logic through the configurable and bypassable PCS interface layers.

The PCS contains multiple gearbox implementations to decouple the PMA and PCS interface widths. The GTS transceiver (PMA with optional FEC or PCS) to FPGA fabric interface support from 8 bits up to 66 bits options. This feature allows you to implement a wide range of applications.

(13) The PCS direct mode is supported on GbE and other protocols.

The PCS hard IP supports various standard and proprietary protocols across a wide range of data rates and encoding schemes.

12.3. GTS Transceiver PLL in Agilex 3 FPGAs and SoCs

There are two types of PLL in the Agilex 3 FPGA GTS transceiver.

Table 18. Types of Agilex 3 FPGA GTS Transceiver PLL

PLL Type	Description
TX PLL	• Four TX PLL per bank or one TX PLL per GTS transceiver channel • LC tank-based PLL with precise fractional synthesis and ultra-low jitter • Supports transceiver interfaces • Dedicated for GTS transceiver usage
System PLL	• One System PLL per bank • Supports only integer mode with precise frequency synthesis • Supports transceiver-to-fabric interfaces • If you do not use the System PLL for the GTS transceivers, you can repurpose this PLL for core fabric usage

13. MIPI Protocols Support in Agilex 3 FPGAs and SoCs

The Agilex 3 FPGAs and SoCs support native MIPI IP D-PHY. The devices support MIPI D-PHY v2.5 at up to 2.5 Gbps per lane. The Agilex 3 FPGAs support MIPI D-PHY high-speed and low-power signaling modes without requiring external components.

Features of the MIPI IP D-PHY:

- Enables unidirectional multi-lane configurations—1, 2, 4, or 8 lanes
- Supports low-power and high-speed signaling up to 2.5 Gbps per lane

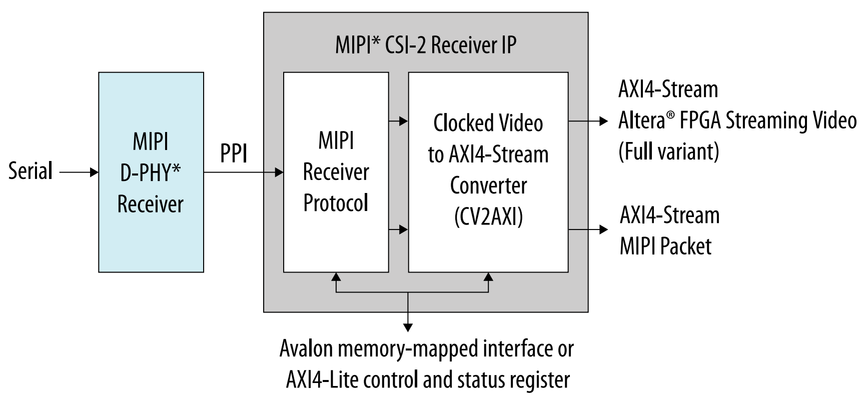
The MIPI IP D-PHY implements MIPI transmit and receive interfaces for Agilex 3 FPGAs in accordance to the following protocols:

- Camera Serial Interface (CSI-2) version 3.0 with underlying D-PHY standard
- Display Serial Interface (DSI-2) version 2.0 with underlying D-PHY standard

Table 19. MIPI CSI-2 and DSI-2 Performance in Agilex 3 FPGAs and SoCs

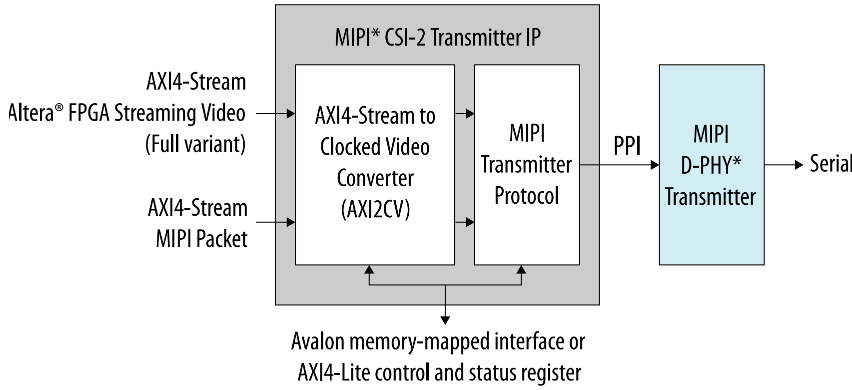
Protocol	C-Series FPGA
CSI-2	• CSI-2 version 3, up to eight lanes • D-PHY v2.5 at up to 2.5 Gbps[(14)]
DSI-2	• DSI-2 version 2, up to four lanes • D-PHY v2.5 at up to 2.5 Gbps[(14)]

Figure 10. MIPI Receiver Block Diagram



(14) Up to 2.5 Gbps for standard reference, short reference, and long reference channels.

Figure 11. MIPI Transmitter Block Diagram

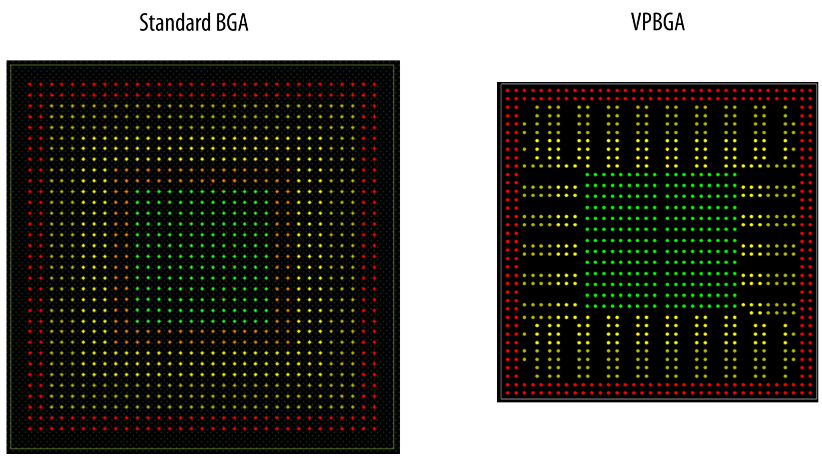


14. Variable Pitch BGA (VPBGA) Package Design of Agilex 3 FPGAs and SoCs

Agilex 3 FPGAs and SoCs packages utilize VPBGA package design and 0.5 mm ball pitch standard ball grid array packaging.

The Variable Pitch BGA (VPBGA) packaging is compatible with Type III PCBs that use the design rules equivalent to 0.8 mm ball pitch and standard plated through hole (PTH) vias. The VPBGA ball pitch is variable and it helps to ease signal routing. For more information, refer to the *PCB Design Guidelines: Agilex 3 FPGAs and SoCs*.

Figure 12. Comparison Between Standard BGA and VPBGA

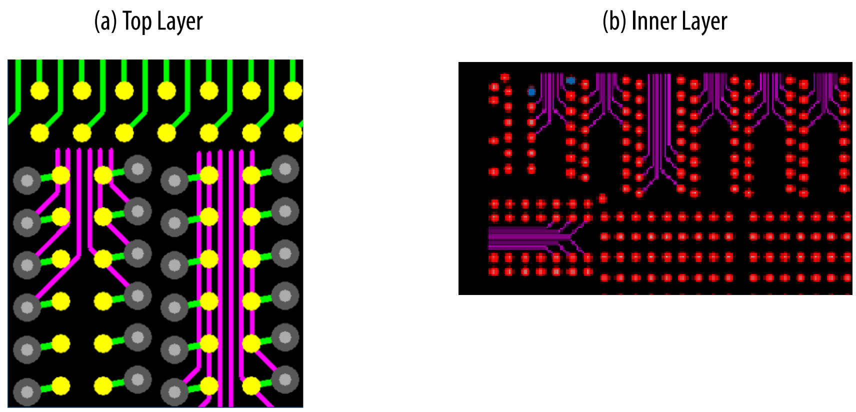


The VPBGA packages with variable ball pitch helps reduce the package form factor. Despite the smaller package size, the VPBGA packages can provide the same I/O pin count and compatible electrical performance compared to the standard BGA packages.

For B18A VPBGA package, the 0.65 mm ball pitch is only available on the two outer rings of the VPBGA package balls, as shown in the top two rows of Figure (a) in the Example of PCB Trace Routing for B18A Variable Pitch BGA (VPBGA) Package figure. The ball pitch is optimized to allow you to route through one signal trace.

Figure (b) in the Example of PCB Trace Routing for B18A Variable Pitch BGA (VPBGA) Package figure shows a wider ball pitch, up to 1.45 mm, which allows you to route through more signal traces compared to standard grid BGA packages. This helps reduce the number of PCB layers—keeping the board cost low with Type III PCBs.

Figure 13. Example of PCB Trace Routing for B18A Variable Pitch BGA (VPBGA) Package



The variable ball grid pattern on the VPBGA packages eases trace routability, reducing the design complexity, number of PCB layers, and board thickness and size—ultimately, reducing board cost and development time.

Note: Information about the B18B and B23C VPBGA packages are under development and not yet available.

15. Configuration via Protocol Using PCIe for Agilex 3 FPGAs and SoCs

Configuration via protocol (CvP) using PCIe allows you to configure the Agilex 3 FPGAs and SoCs across the PCIe bus. This capability simplifies board layout and increases system integration.

The embedded PCIe hard IP operates in autonomous mode before the FPGA is configured. Using this hard IP, you can power up and activate the PCIe bus within the 100 ms time allowed by the PCIe specification.

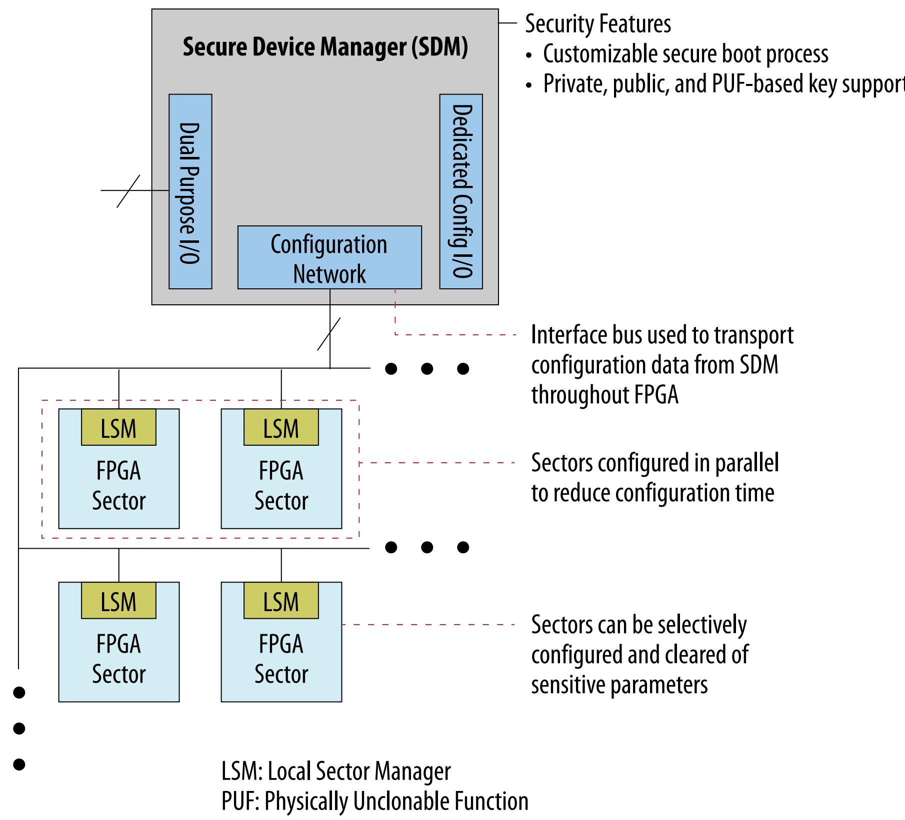
The Agilex 3 FPGAs and SoCs also support partial reconfiguration across the PCIe bus. This capability reduces system downtime by keeping the PCIe link active during device reconfiguration.

16. Device Configuration and the SDM in Agilex 3 FPGAs and SoCs

All Agilex 3 FPGAs and SoCs contain an SDM. The SDM is a triple-redundant processor that serves as the point of entry into the device for all JTAG and configuration commands. Additionally, the SDM in the Agilex 3 FPGAs and SoCs enables system certification to FIPS140-3 layer 2 compliance.

The SDM bootstraps the HPS in Agilex 3 SoCs. This bootstrapping ensures that the HPS boots using the same security features available to the FPGA.

Figure 14. SDM Block Diagram



During configuration, the Agilex 3 FPGA or SoC divides into logical sectors. A local sector manager (LSM) manages each logical sector. The SDM passes configuration data to each LSMs across the on-chip configuration network.

Advantages of the sector-based approach:

- Enables independent configuration of the sectors—one at a time or in parallel
- Achieves simplified sector configuration and reconfiguration
- Reduces overall configuration time caused by inherent parallelism.

The Agilex 3 FPGAs and SoCs use the same sector-based approach to respond to SEUs and security attacks.

Although the sectors provide a logical separation for device configuration and reconfiguration, the sectors overlay the normal rows and columns of FPGA logic and routing:

- No impact to the Quartus Prime software place and route
- No impact to the timing of logic signals that cross the sector boundaries

The SDM enables robust, secure, and fully-authenticated device configuration. Additionally, the SDM allows you to customize the configuration scheme, enhancing device security.

Advantages of the SDM-based device configuration approach:

- Provides a dedicated secure configuration manager
- Reduces device configuration time because sectors are configured in parallel
- Enables an updatable configuration process
- Supports partial reconfiguration
- Allows remote system update
- Supports zeroization of whole device or individual sectors

Table 20. Supported Configuration Schemes for Agilex 3 FPGAs

Configuration Scheme	Data Width	Maximum Data Rate
Active Serial (AS) normal and fast modes	4 bits	4 bits × 166 MHz = 664 Mbps
Avalon streaming interface ×16	16 bits	16 bits × 125 MHz = 2 Gbps
Avalon streaming interface ×8	8 bits	8 bits × 125 MHz = 1 Gbps
JTAG	1 bit	1 bit × 30 MHz = 30 Mbps
Configuration via Protocol (CvP)	×1, ×2, and ×4 lanes	The maximum data rate depends on the PCIe generation and number of lanes. Typically, the data rate of the internal configuration data path of the device, instead of the width of the PCIe link, limits the configuration data width.

17. Partial and Dynamic Configuration of Agilex 3 FPGAs and SoCs

Altera built the partial reconfiguration process on top of the proven incremental compile design flow in the Quartus Prime design software. With partial reconfiguration, you can reconfigure parts of the FPGA while other sections continue to run. In systems with critical uptime requirement, you can update or adjust functions without disrupting service provision.

Apart from lowering power usage and cost, partial configuration effectively increases the logic density. Instead of placing all functions in the FPGA from the start, you can store functions that do not have to operate simultaneously in external memory. You can load these function into the FPGA when needed. Using this technique, you can run multiple applications on a single FPGA and reduce the requirements for FPGA size, board space, and power.

With dynamic reconfiguration, Agilex 3 FPGAs and SoCs can dynamically change data rates, protocols, and analog settings of a transceiver channel without affecting data transfer on adjacent transceiver channels. This capability is ideal for applications that require on-the-fly multi-protocol or multi-rate support.

You can dynamically reconfigure both the PMA and PCS blocks within the transceiver. You can also use dynamic reconfiguration together with partial reconfiguration to partially reconfigure the FPGA core and transceivers simultaneously.

18. Device Security for Agilex 3 FPGAs and SoCs

Agilex 3 FPGAs and SoCs are built with robust security features and managed by the SDM. The devices prioritize the operations of the SDM over fabric and other microprocessor tasks.

The dedicated SDM manages and supports the following critical security features:

- Manages FPGA configuration process and all security features
- Performs authenticated FPGA configuration and HPS boot
- Supports FPGA bitstream encryption, secure key provisioning, and PUF key storage
- Supports platform attestation using the SPDM protocol
- Manages runtime sensors and supports active tamper detection and responses
- Provides user mode access to hardened cryptographic engines as a service

In addition to the preceding list, the following table summarizes the three pillars of security with the advanced security features that Agilex 3 FPGAs and SoCs support.

Table 21. Agilex 3 FPGAs and SoCs Advanced Security Features

Pillar of Security	Device Security Features
Confidentiality, integrity, and availability	• Encryption • Authentication • Attestation • Secure boot • User mode access to cryptographic functions • Secure debug • Vendor authorized boot • Post quantum cryptography (PQC) native boot
Key protection	• Side channel mitigation • Physical anti-tamper detection and response
Secure manufacturing	• Black key provisioning • Secure returned merchandise authorization (RMA)

19. SEU Error Detection and Correction in Agilex 3 FPGAs and SoCs

Agilex 3 devices feature a robust SEU error detection and correction circuitry that protects the configuration RAM (CRAM) programming bits and M20K user memories.

To protect the CRAM, a parity checker circuit runs continuously to automatically correct single-bit or double-bit errors and detect higher order multi-bit errors. The optimized physical layout of the CRAM array makes most multi-bit upsets appear as independent single-bit or double-bit errors. Therefore, the CRAM parity checker circuitry can automatically correct these errors.

The user memories also has integrated ECC circuitry and are also layout-optimized for error detection and correction.

To provide a complete SEU mitigation solution, a soft IP and the Quartus Prime software support the SEU error detection and correction hardware. The following components make up the complete solution:

- Hard error detection and correction for CRAM and M20K user memory blocks
- Optimized memory cells physical layout to minimize the probability of an SEU
- Sensitivity processing soft IP that reports if a CRAM upset affects a used or unused bit
- Fault injection soft IP with Quartus Prime software support to change CRAM bits state for testing
- Hierarchy tagging feature in the Quartus Prime software
- Triple modular redundancy (TMR) for the SDM and critical on-chip state machines

Agilex 3 FPGAs and SoCs also support the following SEU mitigation features:

- Fast SEU detection notification through an IP that connects the LSM pin to the fabric. This notification allows the fabric soft logic to detect reported SEU events faster. You can then retrieve further SEU details through the SDM mailbox.
- External scrubbing for SEU errors that are not automatically correctable. You can create scrubbing bitstream—up to one sector granularity—to scrub the SEU-corrupted configuration bits while keeping the remaining parts of the device intact.
- Single-bit ECC injection, ECC error detection, and reporting on memory in the configuration system. You can test the ECC detection logic by issuing ECC injection commands and querying the ECC status from the SDM.

Furthermore, Agilex 3 FPGAs and SoCs are built on the FinFET-based Intel 7 technology. FinFET transistors are less susceptible to SEUs compared to conventional planar transistors.

20. Power Management for Agilex 3 FPGAs and SoCs

The Agilex 3 FPGA product family offers standard power devices that support fixed core voltage devices with limited core speed options.

The Agilex 3 FPGAs and SoCs C-Series achieve significant total power reduction of up to 38% compared to Cyclone V FPGA.

To achieve the total power reduction, the Agilex 3 FPGAs and SoCs capitalizes on:

- Advanced Intel 7 technology
- Second generation Hyperflex core architecture
- Fixed core voltage
- Other power reduction techniques such as power island and power gating

Table 22. Agilex 3 FPGAs and SoCs C-Series Power Options

Device Type	Description
Fixed voltage	• The devices support 0.75 V and 0.78 V. • Using a fixed low core voltage, the devices further reduce the total power consumption while maintaining device performance.

The power island and power gating feature powers down unused resources in Agilex 3 devices to reduce static power consumption. During configuration, the Quartus Prime software automatically powers down specific unused resources such as the DSP or M20K blocks.

Furthermore, Agilex 3 devices feature industry-leading low power transceivers and include a number of hard IP blocks. The hard IP blocks not only reduce logic resources utilization but also deliver substantial power savings compared to soft implementations. The hard IP blocks generally consume up to 50% less power than equivalent soft logic implementations.

21. Software and Tools for Agilex 3 FPGAs and SoCs

The Quartus Prime Pro Edition design suite supports the Agilex 3 FPGAs and SoCs with a new compiler and the Hyper-Aware design flow.

Together with the Altera oneAPI toolkit, software developers can develop acceleration solutions using Agilex 3 FPGAs and SoCs. The Altera oneAPI toolkit provides a unified, single-sourced, software-friendly, and heterogeneous programming environment for a diverse set of computing engines. The toolkit includes a comprehensive and unified portfolio of developer tools you can use to map software to hardware and accelerate your code.

To improve the efficiency and quality of your designs, Altera also provides the following tools for the Agilex 3 FPGAs and SoCs:

- Transceiver toolkit
- Platform Designer IP integration tool
- Altera DSP Builder for Altera FPGAs advanced blockset
- Arm Development Studio for Altera SoC FPGA (Arm DS for Altera SoC FPGA)

22. Revision History for the Agilex 3 FPGAs and SoCs Device Overview

Document Version	Changes
2025.09.30	• Updated *Agilex 3 FPGAs and SoCs Summary of Features*. • Updated the following tables: — Table: *C-Series FPGA Family Plan—Core Features* — Table: *C-Series FPGA Family Plan—I/Os and Interfaces* — Table: *C-Series FPGA Family Plan—Transceivers and HPS* • Updated the M12A package information for the A3C 025, A3C 050, and A3C 065 devices in Figure: *Package Options, Migrations, and I/O Pins—C-Series*. • Updated the specification, density, and package code information in Figure: *Agilex 3 FPGAs and SoCs Ordering Part Number*. • Updated the cache memory information in Table: *Summary of Agilex 3 SoCs Key Features*. • Updated mentions of TDS to clarify that TDS is LVDS compatible. • Updated the peak theoretical TOPS information for the Agilex 3 FPGAs and SoCs C-Series in *Variable-Precision DSP in Agilex 3 FPGAs and SoCs*. • Updated document for the latest branding standards.
2025.04.22	• Updated mention of cryptography to Cryptographic Services. • Updated the note about the MIPI D-PHY interface in Table: Agilex 3 FPGAs and SoCs C-Series and Table: *Agilex 3 FPGAs and SoCs Summary of Features*. • Updated the number of general purpose I/Os available for Agilex 3 FPGAs and SoCs in Table: *Agilex 3 FPGAs and SoCs Summary of Features*. • Updated the HPS and PCIe descriptions in Table: *Agilex 3 FPGAs and SoCs Summary of Features*. • Updated Table: *C-Series FPGA Family Plan—Transceivers and HPS*. • Updated Figure: *Package Options, Migrations, and I/O Pins—C-Series*: — Updated the number of VPBGA pins in the B23C package pin from 875 to 931. — Added the LVDS pair counts. • Updated Figure: *Agilex 3 FPGAs and SoCs Ordering Part Number*. • Updated Figure: *Agilex 3 SoCs HPS Block Diagram*. • Updated Table: *Summary of Agilex 3 SoCs Key Features*. • Updated the footnote for HSIO's MIPI D-PHY in Table: *I/O Standards Support and Performance*. • Updated the *SEU Error Detection and Correction in Agilex 3 FPGAs and SoCs* topic.
2024.09.23	Initial release.